REMARKS/ARGUMENTS

The Examiner's Action of March 28, 2003, has been received and reviewed by counsel for Assignee. In that Action the Examiner rejected claims 11 and 13-26 based upon prior art references to *Andreev*, U.S. Patent 6,182,272, in view of *Josephson*, U.S. 6,532,580. Other claims were also rejected based upon *Zhen*, U.S. 6,298,468, in view of *Dangelo, et al.*, U.S. 5,880,971. By this response counsel has canceled all pending claims and submits herewith new claims which are believed to patentably distinguish all of the references, either taken separately or combined.

The claimed invention is first discussed below, followed by a discussion of the differences between that and the references.

The Claimed Invention

Claim 32 typifies the steps in Applicant's invention. As shown there, the first two steps of the method result in the creation of a physical layout for a sub-circuit (that is, a circuit having at least 300 gates). The layout includes information to define the physical position of all the components of the circuit, e.g., transistors and interconnections.

Importantly, however, the electrical interconnections among all of the components of the sub-circuit are defined on fewer than all of the layers available for the provision of interconnections on an integrated circuit. In other words, if the integrated circuit provides the capability for four layers of metal interconnections, the electrical connections among the components of the sub-circuit will be defined on no more than three such layers. The sub-circuit is then optimized and stored for later use.

Next, the sub-circuits are utilized in laying out an integrated circuit. Importantly, the interconnections among the sub-circuits, however, are provided entirely on layers other than the layers used for electrical interconnections among the components.

This design technique provides the ability to optimize the performance, power consumption, speed, etc., of a particular sub-circuit and then maintain that sub-circuit in unchanged form for use in a larger integrated circuit. This is beneficial in a sense that when the

larger integrated circuit is created, it is not necessary to design all of the circuitry within it. Instead, to the extent portions of the circuit are designed by the preceding steps, there is no need to redesign them for incorporation into the integrated circuit. By providing the connections within a sub-circuit entirely on separate layers from the connections among sub-circuits, the timing, performance, power, etc., characteristics of a particular sub-circuit will not be impacted by the provision of other sub-circuits. In the prior approaches typified by many of the references cited here, the wiring is not so carefully separated, resulting in poor performance, or unpredictable performance. This results because if the wiring is mixed such that any particular interconnection among any two points in the integrated circuit can be on any arbitrary layer of the integrated circuit, unpredictable wiring paths result, degrading timing, power, etc., performance.

Generally, Applicant's same concept, however, in apparatus form, is claimed in new independent claim 42. This claim is directed to the same feature of providing the sub-circuit connections on fewer than all of the integrated circuit layers. Independent claim 45 also addresses the concept of creating sub-circuits, and the need for providing appropriate interface signals with the sub-circuits. Independent claim 56 is also a general claim relating to the beneficial aspects of designing integrated circuits using the sub-circuit concepts of Applicant herein.

The Prior Art

With respect to the prior art, the *Andreev* reference teaches away from the technique herein. *Andreev* appears to be primarily providing a technique for routing interconnections in integrated circuits, typically gate arrays. As noted by the Examiner, however, *Andreev* does not teach providing intra sub-circuit connections entirely on fewer than all of the layers of the integrated circuit. For this feature the Examiner has relied upon *Josephson*. *Josephson* (and *Block, et al.*, U.S. 6,397,375, commonly assigned with common inventors) each describe a situation in which routing for various layers can be on any layer. For example, in *Josephson* at column 4, lines 45-67, a situation is described in which tracks are set aside specifically for use in conjunction with communications with other layers. For example, as

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described in column 4, beginning at line 45, regions appear to be set aside in each metal layer for repeaters. Whether repeaters are actually placed in those locations will apparently depend upon the particular circuit being designed as to whether a repeater is required or not. As discussed above, however, this presents a significant disadvantage to the design of circuits employing such an approach. The power, timing, etc., performance of such circuits will change depending upon whether the repeaters are provided or are not provided. Applicant's structure, however, maintains the sub-circuit in its original designed form without modification, regardless of the rest of the integrated circuit into which it is introduced.

As a further example, note that in Figure 3 of *Josephson* the timing of each "net" is extracted and prioritized so that the highest priority net can be chosen and a repeater assigned to that net. This is a further indication of the changes which can occur to the design of the integrated circuit, and the potential of changing the timing, power consumption, etc., of a sub-circuit. An important aspect of Applicant's invention is that once the sub-circuits are designed and optimized, they are not changed. This assures predictable performance for each sub-circuit.

An article from EETimes discussing Applicant's unique approach is attached.

CONCLUSION

In view of the foregoing, Applicant believes all claims now pending in this application are in condition for allowance, and an Action to that end is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, he is invited to telephone the undersigned at 650-326-2400.

Respectfully submitted,

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ASIC startup rethinks coarse-grained architectures

By Ron Wilson, EE Times
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URL: http://www.eetimes.com/story/OEG20021022S0017

SAN MATEO, Calif. — Fabless startup Telairity Semiconductor Inc. (Sunnyvale, Calif.) joins the growing list of vendors offering some form of coarse-grained ASIC architecture, but with a significant twist.

Telairity's approach differs from other players such as AMI Semiconductor, NEC Electronics, Chip Express, Lightspeed Semiconductor and eASIC, each offering products that share an important concept with conventional gate arrays and FPGAs. The foundations of their chip — their transistors, contacts and first few metal layers — can be fabricated ahead of time and warehoused. Then a customer's design is fitted into the chip's logic cells, the cells are characterized and interconnected by fabricating the upper metal layers. Like gate arrays, this gives users an advantage in nonrecurring engineering costs and fab turnaround time.

But the biggest potential advantage of the coarse-grained approach is not in the ability to do masterslices. The opportunity is to have a designer reduce a design to basic building blocks in the first place, rather than going through C, Verilog, gate-level netlists and then trying to infer basic blocks. This latter approach can save a great deal of synthesis time. More important, it sharply reduces the amount of time spent on iterations for timing closure, because it meets the all-important metric of keeping the interconnect delay much shorter than the basic block delay.

Larger blocks

This is in effect the Telairity approach. Rather than use configurable basic blocks that are pre-implemented in silicon in fixed locations, Telairity proposed in essence a cell-based design flow in which the cells are not the usual denizens of an ASIC cell library, but much larger blocks averaging about 1,000 equivalent gates, and called groups.

Instead of leaping from a behavioral description to RTL to gates, the Telairity flow uses a proprietary tool to recapture the behavioral design as a connected list of these groups. The flow currently assumes the behavioral description is in Verilog or C++, and assists a designer in manually mapping functional units of code into the predefined groups, using a graphical user interface.

Telairity takes the list, drives the implementation down to the transistor level using its internal definitions of the groups, which are in essence hard macros, and uses a conventional tool flow to place the groups and perform inter-group routing. The flow can be handled either as an ASIC-like flow with a clean handoff to Telairity, or as a

COT-like flow in which a design team stays involved as the groups are placed, routed and the physical design is analyzed.

Group integrity

Telairity has defined the basic blocks or groups to be small physically: about 100 microns on a side in the initial 0.18-micron process. Most of the groups contain only combinatorial logic. Each of these basic blocks is surrounded by a wrapper, called a trailer, that contains whatever input and output registers are required for the function, plus clock distribution and scan chains. The wrappers enforce important standards, including testability, synchronous behavior and consistent contact pitch and location. They also include buffers for use in controlling delay in long interconnect lines that pass over the groups.

Timing within each group is completely characterized when the block is put into the library, and the groups are thoroughly wrung out for signal integrity, design rules and so forth. All have Spice models.

They completely use up metal levels one through three and permit no through-routing on these levels. So, in effect, the most difficult parts of cell-based design have been pushed up to only the higher levels of interconnect.

This approach simplifies the problems of clock and scan insertion. Telairity contends that good placement of these basic blocks will also sharply reduce the design effort required for signal integrity and timing closure.

The bottom line for Telairity is that the methodology, combined with their predefined libraries of functions — each function composed of a list of groups — can sharply reduce design time for a given level of performance. The company doesn't claim a big advantage for designs that are nowhere close to the edge. But as a design begins to push the envelope for speed in a given process — 400 MHz at 0.18 micron, for instance — Telairity claims that its approach gives huge savings in the time required to achieve closure: up to a factor of two, according to president and CEO Howard Sachs.